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BEYER WEAVER LLP
ATTN: ALTERA
P.O. BOX 70250
OAKLAND, CA 94612-0250

EXAMINER
GEBRESILASSIE, KIBROM K

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
Office Action Summary	10/646,193	BAIN, PETER
	Examiner	Art Unit	
	Kibrom K. Gebresilassie	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>23 February 2007</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-57* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *37 and 49* is/are allowed.

6)☒ Claim(s) *1-8,11-20,23-32,35,36,38-48 and 50-57* is/are rejected.

7)☒ Claim(s) *9,10,21,22,33 and 34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

1.   This communication is responsive to amended application filed on February 23,

2007.

2.   Claims 1-57 are pending.

3.   Claims 40-57 are added.

Response to Arguments

4.   <u>Response 112(2) rejection</u>: Applicants are amended the claims to overcome the

rejection and therefore the rejection is withdrawn.

5.   <u>Response to Double Patenting rejection:</u> Applicants indicated that a Terminal

disclaimer was included with the response.

> The Office action has rejected claims 1, 13, 25 and 39 under the judicially-created
> doctrine of obviousness-type double patenting in view of claims 1, 13, 24 and 34 of U.S. Patent
> No. 7,107,567. To obviate the provisional double patenting rejection, <u>Applicant has included a</u>
> <u>terminal disclaimer pursuant to 37 C.F.R. §1.321.</u> Applicant therefore respectfully requests that
> the double patenting rejection be withdrawn.

However, the Terminal disclaimer was not available at the time of examination of

the response filed on February 23, 2007. Therefore, examiner called applicants and

applicants faxed a copy of terminal disclaimer on May 8, 2007, <u>which at the moment is</u>

<u>in process</u>. It is unknown whether the terminal disclaimer is valid or invalid at this

moment and therefore the double patenting rejection is maintained until the terminal

disclaimer is approved (See: ***Double Patenting Rejection*** below).

6.   <u>Response to 101 rejection:</u> Applicants are amended the claims to overcome the

101 rejection and therefore the rejection is withdrawn. However, upon further

consideration, a new ground of rejection is made (See: *Claim Rejections - 35 USC §*

101).

7.   Response 102 rejection: Applicant's arguments filed February 23, 2007 have

been fully considered but they are not persuasive.

> a.   Regarding Claim 39:

Applicants argued:

> Claim 39 requires "a programming version of the IP core for insertion in an electronic
> design." Respectfully, it is pointed out that paragraph 73 of *Meyer* only discloses distribution of
> an IP simulation model. There is no discussion of a programming version of the IP core. As
> discussed at various places in the present application, a programming version is different from a
> simulation model because the programming version may be used to program a programmable
> logic device with an electronic design. The simulation model discussed in *Meyer* at paragraphs
> 72 in 73 cannot be used to program a logic device; therefore, it is not "a programming version of
> the IP core" as required by claim 39.

Examiner respectfully disagrees. In order to have a simulation model of IP core, it

should have the programming version of IP core. Without having a programming version

of the IP core, it is impossible to have the simulation model of IP core.

Applicants argued:

> In other words, the obfuscation circuitry prevents compilation of the simulation model
> into a practical implementation. By contrast, paragraph 72 of *Meyer* does not disclose any
> obfuscation circuitry added to the simulation model that prevents a practical hardware
> implementation. Paragraph 72 does point out that the object code is shrouded or obfuscated, but
> there is no disclosure of any added circuitry. The circuitry of the simulation program of
> paragraph 72 is the original circuitry with no added obfuscation circuitry. The object code is
> apparently obfuscated via different technique. Therefore, this second element of claim 39 is not
> taught or suggested by *Meyer* and it is requested that the rejection of claim 39 be withdrawn.

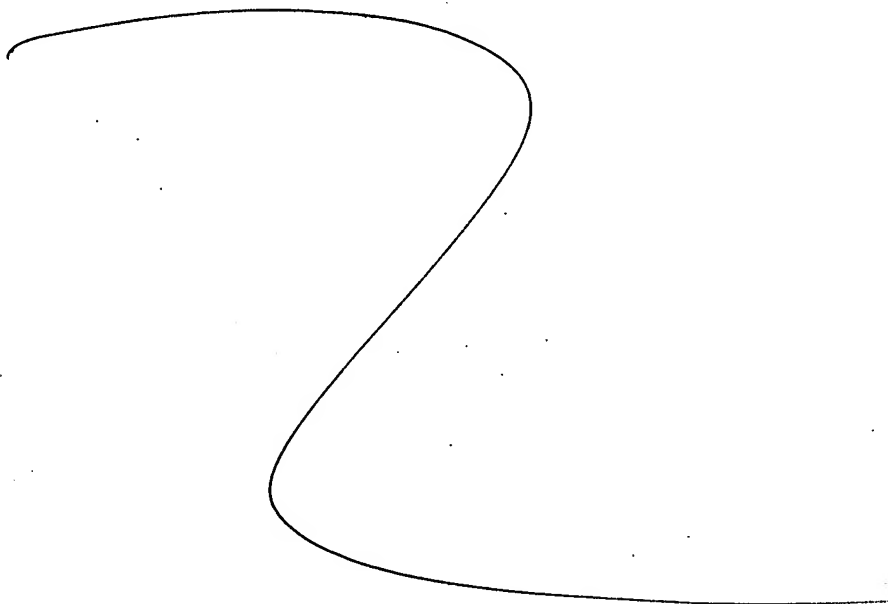Examiner respectfully disagrees. The prior art of reference teaches:

determined by dis-assembly of the simulation program. IP protection is generally superior to any simulator specific model compiler because a simulator vendor does not know the details of the converted library object code and because , which is analogous to prevent direct

compilation of the simulation model.

determined by dis-assembly of the simulation program. IP protection is generally superior to any simulator specific model compiler, because a simulator vendor does not know the details of the converted library object code and because the model compiler vendor is able to shroud and/or obfuscate the object code without increasing simulator development difficulty.

The IP protection such as obfuscation is added to the object code by compiler

vendor. Therefore, the simulator vendor does not know the detail of the converted

object code as stated above.

Further, applicants also admitted that the objected code is already obfuscated via

different technique.

Applicants Own Admission:

paragraph 72 is the original circuitry with no added obfuscation circuitry. The object code is apparently obfuscated via different technique. Therefore, this second element of claim 39 is not

8.   <u>Response 103 rejection:</u> Applicant's arguments filed February 23, 2007 have

been fully considered but they are not persuasive.

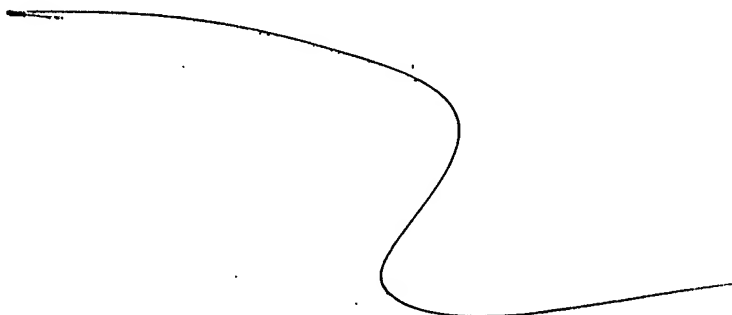   b.   Regarding Claim 1:

Applicants argued:

> Applicant notes from the outset that the present invention is clearly directed toward
> methods and systems used to produce a simulation model of an electronic design in the context
> of programming a programmable logic device using an electronic design automation (EDA)
> system (see page 1). By contrast, *Jakubowski* deals with protecting software from illegal
> copying or modification. <u>There is no disclosure in *Jakubowski* of any EDA systems, electronic
> designs or programmable logic devices.</u> Therefore, is not surprising that many of the claimed
> features of claim 1 are not present in *Jakubowski*.

In response to applicant's argument that the references fail to show certain

features of applicant's invention, it is noted that the features upon which applicant

relies (i.e., EDA systems, programmable logic device) are not recited in the

rejected claim(s). Although the claims are interpreted in light of the specification,

limitations from the specification are not read into the claims. See *In re Van*

Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Further, "electronic design" could be a <u>hardware module design</u> or <u>software</u>

<u>module design</u> or both, which the prior art of reference (Jakubowski et al) teaches a

<u>software module design</u>.

In addition, the prior art of reference (Jakubowski et al) teaches:

> The process is intended to produce a digital good that is
> protected from various forms of attacks and illicit copying
> activities. ~~The obfuscator 134 may be implemented in soft-~~
> ~~ware (or firmware), or a combination of hardware and~~
> ~~software/firmware.~~
, which could be implemented in a

hardware module such as integrated circuits.

c. Applicants argued:

features of claim 1 are not present in *Jakubowski*.

Claim 1 requires as a first step:

receiving a non-obfuscated version of the electronic design suitable for direct
compilation into a practical hardware implementation of the electronic design.
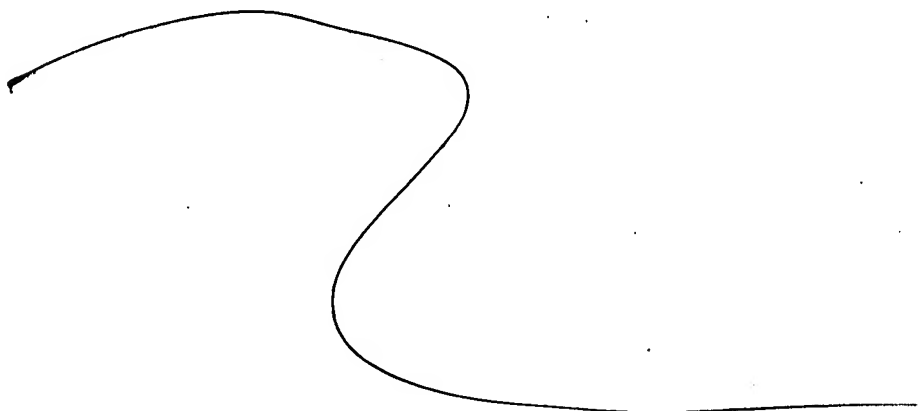
In response, the prior at of reference discloses:

> ~~The original digital good 122 represents the software~~
> ~~product or data as originally produced, without any protec-~~
> ~~tion or code modifications.~~ The protected digital good 124 is
> a unique version of the software product or data after the
> various protection schemes have been applied. The pro-

d. Applicants argued:

Further, this first step of claim 1 requires that the electronic design is suitable "for direct
compilation into a practical hardware implementation." The cited portion of *Jakubowski* (and
the whole reference) does not disclose any software that is suitable for compilation into a
hardware implementation.

It is well known that any unprotected electronic design such as software or
hardware modules could be compile into hardware implementation.

e.   Applicants argued:

> The second step of claim 1 also requires:
>
> wherein said obfuscation circuitry prevents practical implementation of the electronic design on a target hardware device.
>
> Again, *Jakubowski* does not disclose any added circuitry that prevents implementation on a hardware device. The obfuscation techniques of *Jakubowski* might prevent illegal copying, or render illegal copies easily identifiable, but none of the techniques of *Jakubowski* prevent implementation of an electronic design on a hardware device.

In response, the prior art of reference teaches:

> The obfuscator 134 also has a target segment selector 202 that randomly applies various forms of protection to the segmented digital good. In the illustrated implementation, the target selector 202 implements a pseudo random generator (PRG) 204 that provides randomness in selecting various segments of the digital good to protect. The target segment selector 202 works together with a tool selector 206, which selects various tools 136 to augment the selected segments for protection purposes. In one implementation, the tool selector 206 may also implement a pseudo random generator (PRG) 208 that provides randomness in choosing the tools 136.

f.   Applicants argued:

> *Meyer* does disclose in paragraph 96 a simulator that executes system simulation. But, claim 1 requires that the simulation model is created using the obfuscated version of the electronic design. *Meyer* does not teach or suggest a simulation model that is created from an obfuscated version of the electronic design. If anything, the simulation model of *Meyer* is based upon the original electronic design. There is no disclosure in *Meyer* of an obfuscated version of the electronic design that includes added obfuscation circuitry.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Further, The prior art of reference (Meyer et al) teaches the simulation model is created by the obfuscation version of the electronic design. Meyer states as follows:

> determined by dis-assembly of the simulation program. IP protection is generally superior to any simulator specific model compiler, because a simulator vendor does not know the details of the converted library object code and because the model compiler vendor is able to shroud and/or obfuscate the object code without increasing simulator development difficulty.

The underline statement of the prior art states that the obfuscation is already added by a compiler vendor before any simulation is done by the simulation vendor.

g.   <u>Regarding Claim 13, and 25</u>:

The same reasoning for argument will apply as claim 1 above.

h.   <u>Regarding Claim 37</u>:

The rejection of 103(a) has been withdrawn (See: Reason for Allowance below).

i.   <u>Regarding Claim 38</u>:

Applicant's arguments, see Remarks page 22, filed February 2007, with respect to the rejection(s) of claim(s) 38 under 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Koushanfar et al.

Double Patenting

9.　　　The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

　　　A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

　　　Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

　　　Claims 1, 13, 25, and 39 are provisionally rejected on the ground of non-statutory double patenting over claims 1, 13, 24, and 34 of US Patent No. 7,107,567. Although the conflicting claims are not identical, they are not patentably distinct from each other because after analyzing the language of the claims, it is clear that claim 1 of the '567 patent is slightly broader than claim 1 of the instant application. With respect to adding obfuscation circuitry to produce an obfuscated version of the electronic design, the language and the disclosure of the instant application not only fail to distinguish it from the '567 patent, but indicate that it is merely a subset of the '567 patent.

Claims 1, 13, 24, and 34 of Patent No. 7,107, 567 contain every element of claim

1, 13, 25, and 39 of the instant application and thus anticipate the claims of the instant

application. Claims of the instant application therefore are not patently distinct from the

earlier patent claims and as such are unpatentable over obvious-type double patenting.

A later application claims is not patentably distinct from the earlier claim if the later claim

is anticipated by the earlier claim.

Objection to the Specification

10.   The specification is objected to as failing to provide proper antecedent basis for

the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP 608.01(o). Correction of

the following is required: the claims recite a "machine-readable medium" and the

specification does not provide proper antecedent basis for the claimed subject matter.

Although the specification discloses computer readable medium and storage mediums,

the specification does not disclose machine-readable medium. Therefore, the

specification fails to provide proper antecedent basis for the claimed subject matter.

Claim Rejections - 35 USC § 112

11.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter which the applicant regards as his invention.

12.   Claims 1, 13, 25, and 39 are rejected under 35 U.S.C. 112, second paragraph,

as being incomplete for omitting essential steps, such omission amounting to a gap

between the steps. See MPEP § 2172.01. The omitted steps are: **"identifying"** the

region before "adding" an obfuscation circuitry to the electronic design.

13.   Claims 1, 13, 25, and 39 are rejected under 35 U.S.C. 112, second paragraph,

as being incomplete for omitting essential structural cooperative relationships of

elements, such omission amounting to a gap between the necessary structural

connections. See MPEP § 2172.01. The omitted structural cooperative relationships

are: "adding" obfuscation circuitry and "creating" a simulation model. Examiner is

unclear how the "creation" of a simulation model is done.

14.   The term "substantially" in claims 40-45 is a relative term, which renders the

claim indefinite. The term "substantially" is not defined by the claim, the specification

does not provide a standard for ascertaining the requisite degree, and one of ordinary

skill in the art would not be reasonably apprised of the scope of the invention.

15.   Claims 8, and 20 recite the term "and/or". This term renders the claims vague

and indefinite because the term "and/or" is considered to be alternative languages.

Therefore, it is unclear as to how the examiner should interpret the claim limitation as it

relates to "and/or".

Claim Rejections - 35 USC § 101

16.   35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of
> matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the
> conditions and requirements of this title.

17.   Claims 25, and 39 are rejected under 35 U.S.C. 101 because the claimed

invention is directed to non-statutory subject matter.

j.   <u>As per claim 25:</u>

The claimed invention recites a "computer readable medium".

The specification defines:

> Examples of computer-readable media include, but are not limited to, magnetic media such as hard disks, floppy disks, and magnetic tape; optical media such as CD-ROM disks; magneto-optical media; semiconductor memory devices, and hardware devices that are specially configured to store and perform program instructions, such as read-only memory devices (ROM) and random access memory (RAM). The data and program instructions of this invention may also be embodied on a carrier wave or other transport medium (including electronic or optically conductive pathways).

According to the specification, the "computer-readable medium" is not limited to tangible mediums. It could also include non-tangible mediums. Therefore, the "computer-readable medium" is not limited to physical articles or objects which constitute a manufacture with in the meaning of 35 USC 101 and enable any functionality of the instructions carried thereby to act as a computer component and realize their functionality. As such, the claim is not limited to statutory subject matter and is therefore non-statutory.

k.   As per claim 39:

i.   The claimed invention recites a "machine readable medium" and the specification fails to provide antecedent basis for the limitation [See: **Objection to the Specification** above]. Without antecedent basis for "machine readable medium", it is unclear if the limitation intended to be a tangible medium. It is believed that the limitation "machine readable medium" is intended to claim something boarder than a tangible medium and cover signals, waves and other form of transmission media, that carry instruction. Therefore, the "machine readable medium" is not limited to physical articles or objects which constitute a manufacture with in the meaning of 35 USC 101 and enable any functionality of the instructions

carried thereby to act as a computer component and realize their

functionality. As such, the claim is not limited to statutory subject matter

and is therefore non-statutory.

ii.   Further, Claim 39 is rejected under 35 U.S.C. 101 as being directed

to nonstatutory subject matter since the claims as a whole are drawn to

software per se and do not provide for a practical application, as

evidenced by lack of physical transformation or a useful, tangible, and

concrete result.

MPEP 2106 states as follows:

**>Descriptive material can be characterized as either "functional descriptive material" or
"nonfunctional descriptive material."** In this context, "functional descriptive material"
consists of data structures and computer programs which impart functionality when
employed as a computer component. (The definition of "data structure" is "a physical or

When nonfunctional descriptive material is recorded on some computer-readable
medium, in a computer or on an electromagnetic carrier signal, it is not statutory since no
requisite functionality is present to satisfy the practical application requirement. Merely
claiming nonfunctional descriptive material, i.e., abstract ideas, stored on a computer-
readable medium, in a computer, or on an electromagnetic carrier signal, does not make

it statutory. See *Diehr*, 450 U.S. at 185-86, 209 USPQ at 8 (noting that the claims for
an algorithm in *Benson* were unpatentable as abstract ideas because "[t]he sole practical
application of the algorithm was in connection with the programming of a general purpose
computer."). Such a result would exalt form over substance. *In re Sarkar*, 588 F.2d
1330. 1333, 200 USPQ 132, 137 (CCPA 1978) ("[E]ach invention must be evaluated
as claimed; yet semantogenic considerations preclude a determination based solely on
words appearing in the claims. In the final analysis under § 101, the claimed invention, as
a whole, must be evaluated for what it is.") (quoted with approval in *Abele*, 684 F.2d at
907, 214 USPQ at 687). See also *In re Johnson*, 589 F.2d 1070, 1077, 200 USPQ
199, 206 (CCPA 1978) ("form of the claim is often an exercise in drafting"). Thus,
nonstatutory music is not a computer component, and it does not become statutory by
merely recording it on a compact disk. Protection for this type of work is provided under
the copyright law.

I.   All dependent claims are also rejected because they depend on rejected

claims 25, and 39.

Claim Interpretation

18.   As per claims 1, 13, and 25, the claimed invention recites a limitation of "said

simulation model being suitable for producing accurate hardware simulation results in a

simulator but not being suitable to be directly compiled to produce a practical hardware

implementation of the electronic design", which refers to intended use. This limitation is

generally not accorded any patentable weight where it merely recites the purpose of a

process or the intended use of a structure.

19.   As per claim 39, the claimed invention recites a limitation of "which allows an

accurate a hardware simulation result of the IP core but prevents direct compilation of

the simulation model to produce a practical hardware implementation of the IP core",

which refers to intended use. This limitation is generally not accorded any patentable

weight where it merely recites the purpose of a process or the intended use of a

structure.

Claim Rejections - 35 USC § 102

20.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public
use or on sale in this country, more than one year prior to the date of application for patent in the United
States.

21.   Claim 38 is rejected under 35 U.S.C. 102(b) as being anticipated by F.
Koushanfar, and G. Qu, "hardware Metering" 2001 ACM.

As per Claim 38:

Koushanfar discloses a method of producing a simulation model of an intellectual
property core, wherein the simulation model produces a hardware simulation result but
cannot be directly compiled to produce a practical hardware implementation of the IP
core, the method comprising:

(a) receiving a non-obfuscated version of the IP core in a native HDL format or in
a partially compiled HDL format (such as ....*original IP specification during its
creation and/or synthesis...*; **See: page 2, left side column, 22-25**);

(b) identifying a region of the non-obfuscated IP core where one or more flip-flops
are located (such as ...*the algorithms decide exactly where to burn the
interconnect in each chip...*; **See: page 3, left side column, lines 4-12**);

(c) inserting obfuscation circuitry into the region (such as...*IP protection is
based on the constraint manipulation...The basic idea is to impose additional
author specific constraint on the original IP...obfuscation can be used for IP
protection...*; **See: page 2, left side column, lines 22-36**);

(d) adding additional flip-flops and/or modifying the flip-flops (such as...*adding
FSM...*; **See: page 3, left side column, lines 2-5**); and

(e) optimizing the IP core after (c) and (d) have been performed (such as...*GC
optimization...*; **See: "6. Design Flow"**); and

(f) producing a simulation model using said optimized IP core that includes said inserted obfuscation circuitry (**See: page 4 "Conclusion"**).

22.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

23.   Claim 39 is rejected under 35 U.S.C. 102(e) as being anticipated by Publication No. US 2002/0138244 A1 issued to Meyer et al.

As per Claim 39:

Meyer discloses a computer program product comprising a machine-readable medium on which is provided program instructions for implementing an intellectual property (IP) core said program instructions comprising:

a programming version of the IP core for insertion in an electronic design developed using a specified electronic design automation (EDA) platform (**See:** [0073]); and

a simulation model of the IP core for simulating operation of the IP core in the electronic design, wherein the simulation model includes comprises obfuscation circuitry, absent in the programming version, which allows an accurate a hardware simulation result of the IP core but prevents direct compilation of the simulation model to produce a practical hardware implementation of the IP core (**See:**[0072]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

24. Claims 1-5, 7, 8, 11-20, 23-32, 35, 36, 40-42, 44-48, and 50-57 are rejected

under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 7,080,257 issued to

Jakubowski et al in view of Publication No. US 2002/0138244 A1 issued to Meyer et al.

As per Claim 1:

Jakubowski discloses a method of producing model of an electronic design, the

method comprising:

receiving a non-obfuscated version of the electronic design suitable for direct

compilation into a practical hardware implementation of the electronic design (**See: Fig.**

2 element 122 and corresponding texts; Col. 4 line 5-7); and

adding obfuscation circuitry to said electronic design to produce an obfuscated

version of the electronic design, wherein said obfuscation circuitry prevents practical

implementation of the electronic design on a target hardware device (**See: Col. 5 lines 55-64**);

creating model using said obfuscated version of said electronic design said simulation model being suitable for producing accurate hardware simulation results in a simulator but not being suitable to be directly compiled to produce a practical hardware implementation of the electronic design (**See: Fig. 2 element 124 and corresponding texts**); and

storing said simulation model in a computer system (**See: Fig. 1 element 108 and corresponding texts**).

Jakubowski teaches producing of protected digital goods such as software modules. However, Jakubowski is silent whether the protected digital goods are a simulation model results in a simulator.

Meyer discloses a simulation model results in a simulator (such as...*HDL simulator...*; **See: Abstract**).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Meyer et al with Jakubowski et al because both references are clearly concerned with protection of an intellectual property. The motivation for doing so would have been convenient to connect an HDL simulator, as taught by Meyer et al, to verify an electronic design.

As per Claim 2:

Meyer discloses a method as recited in claim 1, wherein the non-obfuscated version of the electronic design is provided in an HDL source format and said creating a

simulation model includes using said obfuscated version of said electronic design as said simulation mode (**See: Abstract, [0072], [0101]**).

As per Claim 3:

Meyer discloses a method as recited in claim 1, wherein the electronic design is a reusable functional logic block (**See: [0026]**).

As per Claim 4:

Jakubowski discloses a method as recited in claim 1, wherein adding Obfuscation circuitry includes comprise: identifying a region for introduction of obfuscation circuitry in the non-obfuscated version of the electronic design; choosing a type of obfuscation circuitry for insertion; and inserting the chosen type of obfuscation circuitry into the identified region, thereby creating an obfuscated region (**See: Fig. 2 element 202 and corresponding texts, Fig. 2 element 206 and corresponding texts, Fig. 4 and corresponding texts**).

As per Claim 5:

Jakubowski discloses a method as recited in claim 4, wherein identifying a region for introduction of obfuscation circuitry includes comprises identifying in the non-obfuscated version of the electronic design logic of a type that is not removed by a synthesizer (**See: Fig. 2 element 202 and corresponding texts**).

As per Claim 7:

Meyer discloses a method as recited in claim 1, further comprising: optimizing the obfuscated version of the electronic design by merging the obfuscation circuitry with non-obfuscated functional circuitry of said obfuscated version (such as...*the preferred*

embodiment has the advantage that optimization and shrouding or obfuscation

operation...; See: [0101]).

As per Claim 8:

Jakubowski discloses a method as recited in claim 1, wherein the obfuscation

circuitry increases the size of the electronic design without changing its function and/or

slows the speed of the electronic design without changing its function (**See: Col. 6 lines**

49-50).

As per Claim 11:

Jakubowski discloses a method as recited in claim 1, wherein the obfuscation

circuitry includes an comprises-a XOR tree (**See: Col. 9 lines 16-23**).

As per Claim 12:

Jakubowski discloses a method as recited in claim 1., wherein adding

obfuscation circuitry is performed automatically without user intervention (**See: Col. 3**

lines 31-33).

As per Claim 13:

Jakubowski discloses an apparatus for producing a model of an electronic

design, the apparatus comprising:

one or more processors (**See: Fig. 1 element 102 and corresponding texts**);

memory (**See: Fig 1 element 120 and corresponding texts**);

a design entry tool that allows a developer to input a non-obfuscated version of

said electronic design (**See: Fig. 1 element 100**);

an obfuscation module for adding obfuscation circuitry to said a non-obfuscated version of the electronic design to produce an obfuscated version of the electronic design from which the model can be created, wherein said obfuscation circuitry prevents practical implementation of the electronic design on a target hardware device **(See: Fig. 2 element 122 and corresponding texts; Col. 4 line 5-7)**, said obfuscation module creating said simulation model, said model being suitable for producing accurate hardware results but not being suitable to be directly compiled to produce a practical hardware implementation of the electronic design (**See: Fig. 2 element 124 and corresponding texts**).

Jakubowski teaches producing of protected digital goods such as software modules. However, Jakubowski is silent whether the protected digital goods are a simulation model results in a simulator.

Meyer discloses a simulation model results in a simulator (such as *...HDL Simulator...*; See: Abstract).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Meyer et al with Jakubowski et al because both references are clearly concerned with protection of an intellectual property. The motivation for doing so would have been convenient to connect an HDL simulator, as taught by Meyer et al, to verify an electronic design.

As per Claim 40:

Jakubowski discloses a method as recited in claim 8, wherein the obfuscation circuitry substantially increases the area of the electronic design or reduces the speed of a critical path of the electronic design (**See: Col. 6 lines 49-50**).

As per Claim 46:

Meyer discloses a method as recited in claim 1 wherein said simulation model is cycle accurate and bit accurate (**See: [0033]**).

As per Claim 50:

Meyer discloses a method as recited in claim 38 further comprising: producing a simulation model using said optimized intellectual property core, wherein said simulation model is cycle accurate and bit accurate (**See: [0033]**).

As per Claim 52:

Meyer discloses a method as recited in claim 3 wherein said functional logic block is an intellectual property core (**See: [0078]**).

As per Claim 55:

Meyer discloses a method as recited in claim 1, wherein the non-obfuscated version of the electronic design is provided in a partially compiled format, and wherein said creating a simulation model includes using a translation utility to convert said obfuscated version of said electronic design into said simulation model having a standard format usable by a variety of simulators (**See: [0073]**).

25.　Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Patent No. 7,080,257 issued to Jakubowski et al in view of Publication No. US 2002/0138244 A1 issued to Meyer et al as applied to claims 1-5, 7, 8, 11-20, 23-32, 35, 36, 40-42, 44-

48, and 50-57 above, and further in view of F. Koushanfar, and G. Qu, "hardware

Metering" 2001 ACM.
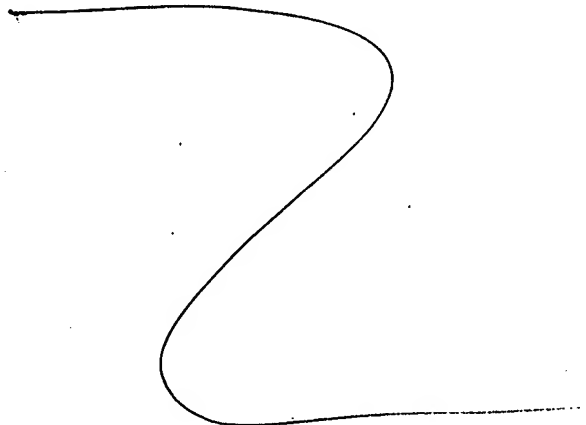
As per Claim 6:

Jakubowski fails to disclose one or more flip-flops.

Koushanfar discloses a method as recited in claim 5, wherein the type of logic

that is not removed by a synthesizer includes comprises one or more flip-flops (such as

...*Finite State Machine...*; See: page 3, left side column, lines 4-5).

It would have been obvious to one of ordinary skill in the art at the time of the

invention was made to combine the teachings of Koushanfar et al with Jakubowski et al

because both references are clearly concerned with protection of an intellectual

property. The motivation for doing so would have been convenient to connect additional

Finite State Machine which comprises a flip-flops, as taught by Koushanfar et al, to

achieve a slightly different control path.

As per Claims 14-20, 23-32, 35, 36, 41-45, 47, 48, 50, 51, 53, 54, 56, and 57:

The limitations of claims 14-20, 23-32, 35, 36, 41-45, 47, 48, 50, 51, 53, 54, 56,

and 57 have already been discussed in the rejection of claims 1-8, 11, 12, 40, 46, 52,

and 55. The instant claims is/are functionally equivalent to the above rejected claims

and is/are therefore rejected under the same rationale.

Allowable Subject Matter

26.   Claims 37, and 49 are allowed.

m.   The following is an examiner's statement of reasons for allowance:

The prior art of reference expressly fails to disclose the limitation of:

As claim 37, *inserting entangler circuitry upstream from the region and inserting complementary detangler circuitry downstream from the region*; and

inserting scrambler circuitry upstream from the region and inserting complementary descrambler circuitry downstream from the region.

As claim 49, it depends on claim 37 and therefore allowed.

27.   Claims 9, 10, 21, 22, 33, and 34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

n.   The following is a statement of reasons for the indication of allowable subject matter:

The prior art of reference expressly fails to discloses the limitation of:

As per claim 9, *adding circuitry for scrambling an input signal by spreading out the input signal in time*; and *adding circuitry for de-scrambling an output signal resulting from the circuitry for scrambling,*

As per claim 10, *adding circuitry for entangling multiple input signals to thereby spread out the input signals; and adding circuitry for detangling an output signal resulting from the circuitry for entangling.*

As per claims 21, 22, 33, and 34, the same statement of reasons will apply as claim 9, and/or 10 because they have similar limitation as claims 9 and/or 10.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."
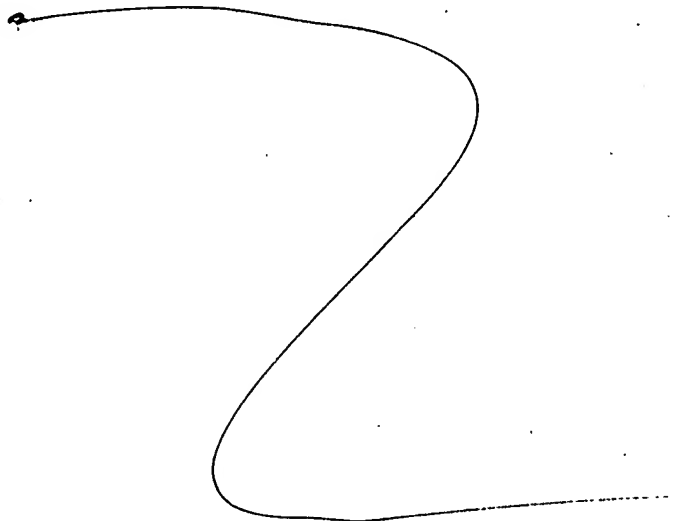
Conclusion

28.   Claims **1-5, 7, 8, 11-20, 23-32, 35, 36, 38-42, 44-48, and 50-57 are rejected.**

29.   Claims 37, and 49 are allowed.

30.   Claims 9, 10, 21, 22, 33, and 34 are objected.

31.   Examiner's Note: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

32.   In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.
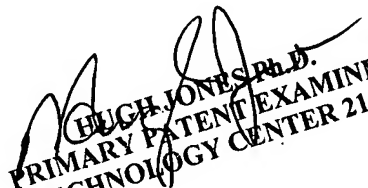
Communications

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kibrom K. Gebresilassie whose telephone number is 571-272-8571. The examiner can normally be reached on 8:00 am - 4:30 pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on 571-272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KG

HUGH JONES, Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100